REMARKS

Claim Objections

In the Office Action, claims 7 and 25 were objected to.

Claim 7 had been amended to conform with the spirit of the Examiner's rejection for both claims 7 and 25 (which depends from claim 7).

Claim Rejections

35 U.S.C. §112

In the Office Action, claims 15-24 were rejected under 35 U.S.C. 112.

The Examiner asserts that the phrase "a same known logic value" renders the claim unclear as to whether the known logic value is zero, one or a value between zero and one. Applicants respectfully assert that this is not unclear. As to a value between zero and one, this implies that the logic value is not known. Thus applicant respectfully submits that a value between zero and one is not a possibility. As to whether the "same known logic value" is a zero or a one, in this claim, the claim is meant to encompass both conditions. That is, a same known logic value could be either a logic "0" or a logic "1". Claim 26 has been added to aide in clarifying this position.

In addition, the Examiner states that the phrase "to facilitate reduction of current drain by reducing contention on outputs of said plurality of output buffers" renders the claim unclear. Claim 15 has been amended to further clarify.

35 U.S.C. §103

In the Office Action, claims 1-14 were rejected under 35 U.S.C. 103.

Sample in view of Agrawal

In the Office Action, claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,289,494 to Sample et al. (hereinafter *Sample*) in view of U.S. Patent No. 5,644,496 to Agrawal et al. (hereinafter *Agrawal*) (Examiners Response A). For the reasons stated below Applicants respectfully submit that claims 1-6 are patentable over *Sample* in view of *Agrawal*.

Claim 1, as amended, reads:

> A crossbar device comprising:
> n input lines;
> m output lines; and
> a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to selectively couple said n input lines to said m output lines, wherein at least one of the plurality of chains of pass transistors comprises a first and a second pass transistor coupled such that said first transistor drives a load consisting essentially of said second transistor and interconnect between said first and said second transistor,
> where n and m are integers.

As asserted by the Examiner, *Agrawal* teaches a programmable interconnect point **521** coupled to a MUX **501**. The Examiner asserts that utilizing the MUX structure of *Sample* (FIG 13D) as the MUX in *Agrawal* renders claim 1 obvious. Applicants respectfully disagree. Nevertheless, Applicants have amended claim 1 to further distinguish claim 1.

As illustrated in *Agrawal*, the PIP **521** drives a number of muxes. This is apparent as the connection between the PIP **521** and the mux **501** is via a long line **520**. As noted in the paragraph beginning on line 66 of column 13, "Each IOB has a least one input supplied from a 'committed' long line (e.g. 520) ...". Thus, the PIP **521** drives a number of IOBs, each IOB having a mux **501**. In contrast, the first transistor of the

chain of transistors above, drives a load consisting essentially of a second transistor and interconnect between the first and second transistors.

Additionally, Applicants do not agree with Examiners discussion of the reason for the PIP 521. The Examiner states that PIP **521** is "to control timing for selectively feeding appropriate data into the cross device thereby improving the performance of the crossbar device." Respectfully, Applicants were not able to determine where *Agrawal* so characterizes the PIP **521**. However, this point is not germane to the claims as pending.

For at least the reasons discussed above, Applicants respectfully submit that claim 1 is patentable over *Sample* in view of *Agrawal*.

Claims 2-6 depend from independent claim 1 incorporating its limitations. Thus, by virtue of at least their dependency on claim 1, claims 2-6 also recite patentable subject matter.

Sample in view of Patel and Admitted Prior Art

In the Office Action, claims 7, 13 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art and U.S. Patent No. 6,175,952 to Patel et al. (hereinafter *Patel*). For the reasons stated below Applicants respectfully submit that claims 7, 13 and 14 are patentable over *Sample* in view of *Patel* and admitted prior art.

Claim 7 reads:

A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically associated with the memory element; and

a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

Sample and the admitted prior art does not teach a voltage supply structure as recited in the claim 7. The Examiner states that *Patel* teaches this subject matter in FIGs 23. Applicants respectfully disagree.

The Examiner states that the cross coupled latch is an output buffer. Applicants respectfully disagree. The cross coupled latch is a pair of cross coupled inverters designed to perform a latch function and an inversion function vis-à-vis a buffer function. The output 2333 is the logical inversion of the input 2331. Moreover, the feedback from inverter 2335 provides a memory feature. Thus device is a sequential (e.g. memory) device which inverts the logic value and not a buffer.

Moreover, as previously stated, the disclosure in Figure 23 illustrates the use of separate supply voltage in isolation device **2315** to **protect circuitry connected to the output of isolation device 2315**. The protected circuitry uses VCC1. The isolation device uses VCC2. The isolation device is intended to prevent high voltages from damaging downstream circuitry **2310** that would otherwise be driven by the signal driving the isolation device **2321** (column 26, lines 39-42). Thus, in *Patel,* the circuitry is designed to prevent higher voltages from being passed to the second stage. The circuitry is not designed to maintain the input voltage of the output buffers at Vdd.

The Examiner also states that

> Patel et al. also teach that, in order to achieve (i.e. maintain) output signal at a desired Vcc (i.e., Vdd) level, the bias supply voltage (Vcc2) of a pass-transistor of output switch should be at about Vcc + |Vth| level, where |Vth| is a threshold voltage.

Applicants respectfully disagree. Patel discusses, in the cited sections col 13 lines 36-44 and 61-63, a design where sneak currents I1 and I2 (as illustrated in FIG 8) can be prevented when a voltage above a supply voltage is place at a pin to a design. Col 14 lines 17-19). The various discussions related to FIG 10A, including the cites of col 13 lines 36-44 and 61-63, are related to the various operating modes of the circuit of FIG 10A. These operating modes discuss the operation of the circuit when the voltage on pin **820** ranges from ground to above Vcc. Included in that is a discussion of the operation of the circuit when the voltage is in the ground to Vcc – Vth region col 13 lines 36-44. However, this section does not disclose a voltage raised by a threshold over Vdd to memory elements to maintain an input voltage of the output buffers at Vdd.

In addition, the Examiner states that "It is indicated in FIG. 1b of applicants admitted prior art that the supply voltage of pass transistor is coupled from a memory element." Applicant respectfully disagree. FIG. 1b of applicants admitted prior art illustrates a pass transistor **103** whose gate is controlled by a memory element **104**. Thus there is no disclosure/discussion related to FIG 1b that the **supply voltage** of pass transistor is coupled from a memory element. It is the gate that is coupled to the memory element.

Thus, for at least the reasons discussed above, Applicants respectfully submit that claim 7 is patentable over *Sample* in view of *Patel* and admitted prior art.

Claims 13-14 depend from independent claim 7 incorporating its limitations. Thus, by virtue of at least their dependency on claim 7, claims 13-14 also recite patentable subject matter.

Sample in view of Patel, Agrawal and Admitted Prior Art

In the Office Action, claims 8-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art, *Patel* and *Agrawal*. For the reasons stated below Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of *Patel, Agrawal* and admitted prior art.

Claims 8-12 depend from claim 7. In addition to the limitations of claim 7, these claims contain additional limitations substantially similar to claim 1. *Patel* does not solve the deficiencies of the previous arguments with respect to claim 1. In addition, *Agrawal* does not solve the deficiencies of the previous arguments with respect to claim 7. Thus, for at least the reasons set forth with respect to both claim 1 and claim 7 above, Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of admitted prior art, *Patel* and *Agarwal*.

Conclusion

In view of the forgoing, Applicants respectfully submit that claims 1-26 are in condition for allowance. Early issuance of the Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
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